

# FDB52N20

## 200V N-Channel MOSFET

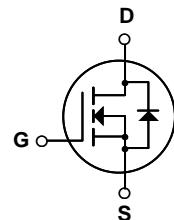
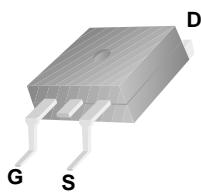
### Features

- 52A, 200V,  $R_{DS(on)} = 0.049\Omega$  @  $V_{GS} = 10$  V
- Low gate charge ( typical 49 nC)
- Low  $C_{rss}$  ( typical 66 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



### Absolute Maximum Ratings

Symbol	Parameter	FDB52N20	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	52 33	A A
$I_{DM}$	Drain Current - Pulsed	(Note 1)	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	357 2.86	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB52N20	FDB52N20TM	D <sup>2</sup> -PAK	330mm	24mm	800

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

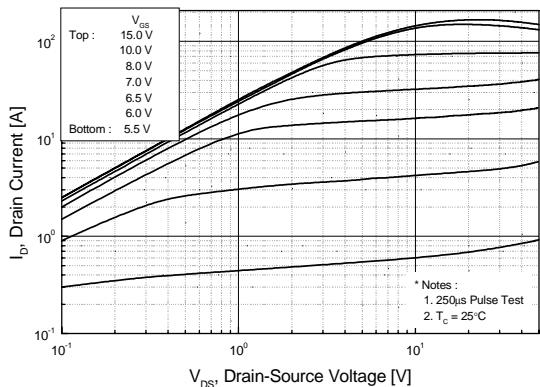
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$	200	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.2	--	$\text{V}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 200\text{V}$ , $V_{\text{GS}} = 0\text{V}$ $V_{\text{DS}} = 160\text{V}$ , $T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{\text{GSSF}}$	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30\text{V}$ , $V_{\text{DS}} = 0\text{V}$	--	--	100	nA
$I_{\text{GSSR}}$	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30\text{V}$ , $V_{\text{DS}} = 0\text{V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$	3.0	--	5.0	V
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10\text{V}$ , $I_D = 26\text{A}$	--	0.041	0.049	$\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 40\text{V}$ , $I_D = 26\text{A}$	(Note 4)	35	--	S
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 25\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $f = 1.0\text{MHz}$	--	2230	2900	pF
$C_{\text{oss}}$	Output Capacitance		--	540	700	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		--	66	100	pF
<b>Switching Characteristics</b>						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 100\text{V}$ , $I_D = 52\text{A}$ $R_G = 25\Omega$	--	53	115	ns
$t_r$	Turn-On Rise Time		--	175	359	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	48	107	ns
$t_f$	Turn-Off Fall Time		--	29	68	ns
$Q_g$	Total Gate Charge	$V_{\text{DS}} = 160\text{V}$ , $I_D = 52\text{A}$ $V_{\text{GS}} = 10\text{V}$	--	49	63	nC
$Q_{\text{gs}}$	Gate-Source Charge		--	19	--	nC
$Q_{\text{gd}}$	Gate-Drain Charge		--	24	--	$\mu\text{C}$
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	52	--	A
$I_{\text{SM}}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	204	--	A
$V_{\text{SD}}$	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_S = 52\text{A}$	--	--	1.4	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_{\text{GS}} = 0\text{V}$ , $I_S = 52\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$	--	162	--	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		--	1.3	--	$\mu\text{C}$

### NOTES:

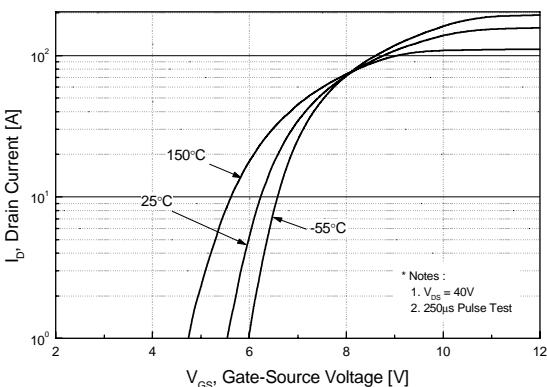
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 1.4\text{mH}$ ,  $I_{AS} = 52\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 52\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq \text{BV}_{\text{DSS}}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

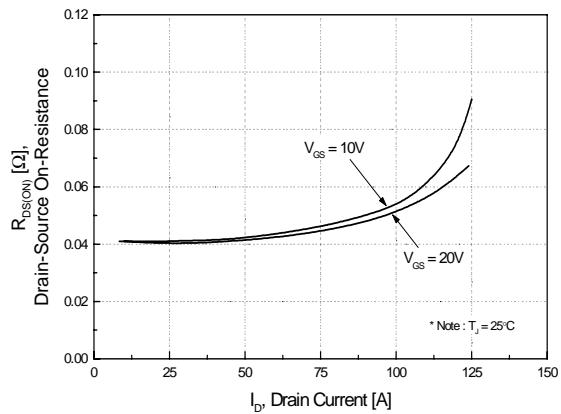
**Figure 1. On-Region Characteristics**



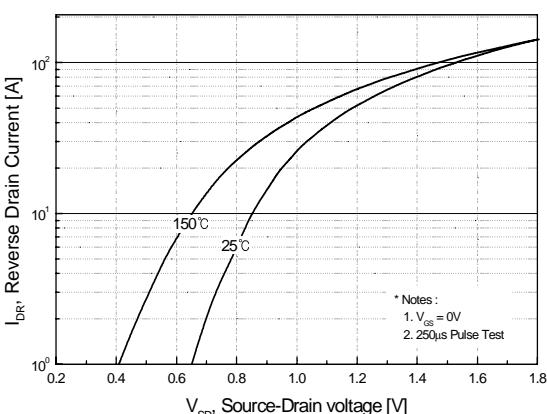
**Figure 2. Transfer Characteristics**



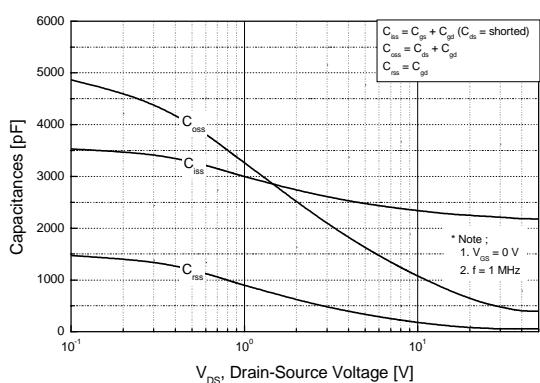
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



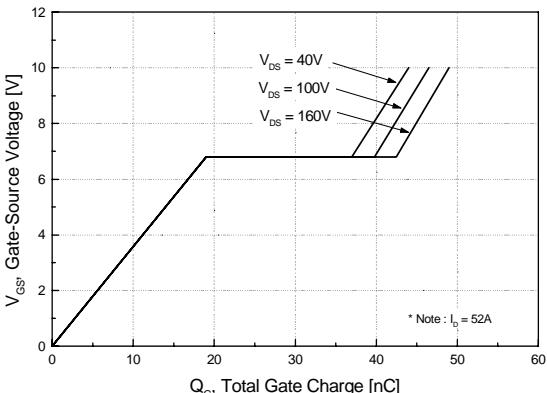
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

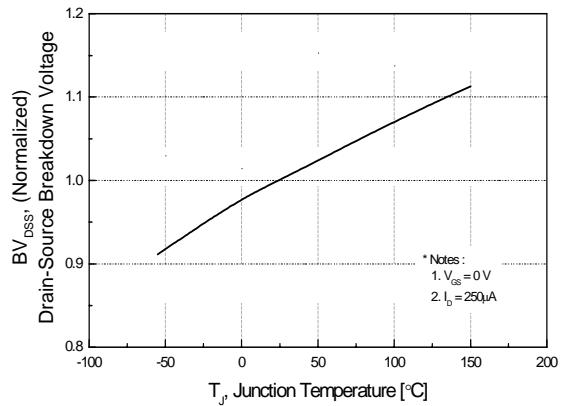


**Figure 6. Gate Charge Characteristics**

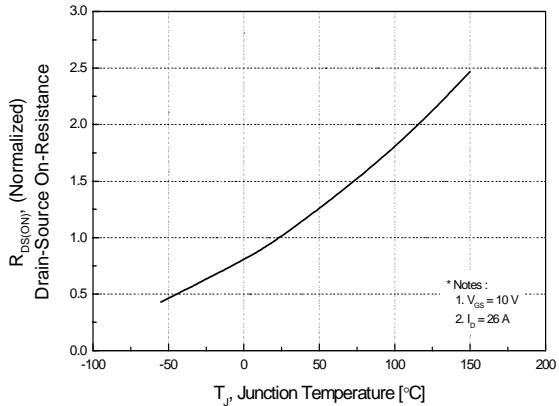


## Typical Performance Characteristics (Continued)

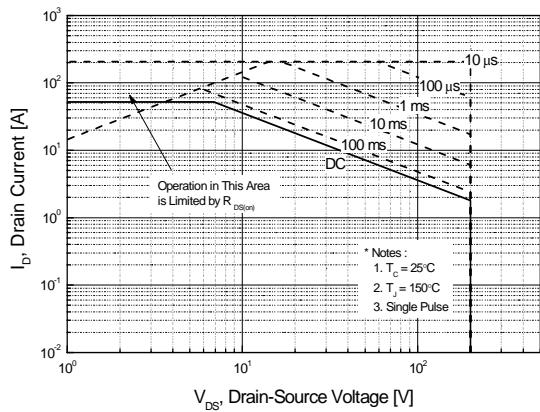
**Figure 7. Breakdown Voltage Variation vs. Temperature**



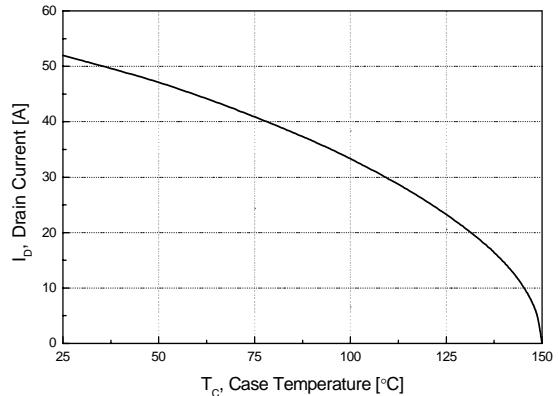
**Figure 8. On-Resistance Variation vs. Temperature**



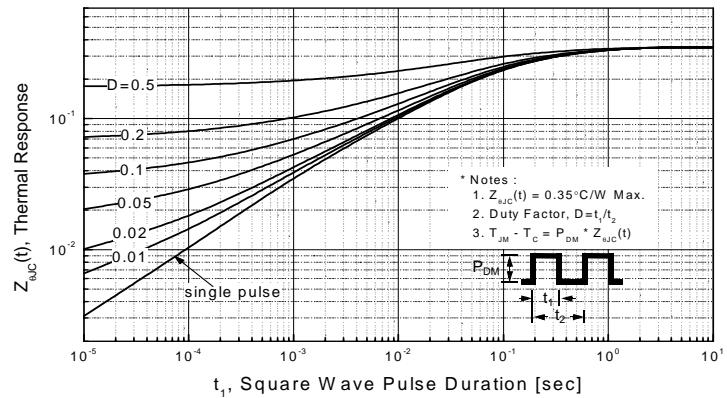
**Figure 9. Maximum Safe Operating Area**



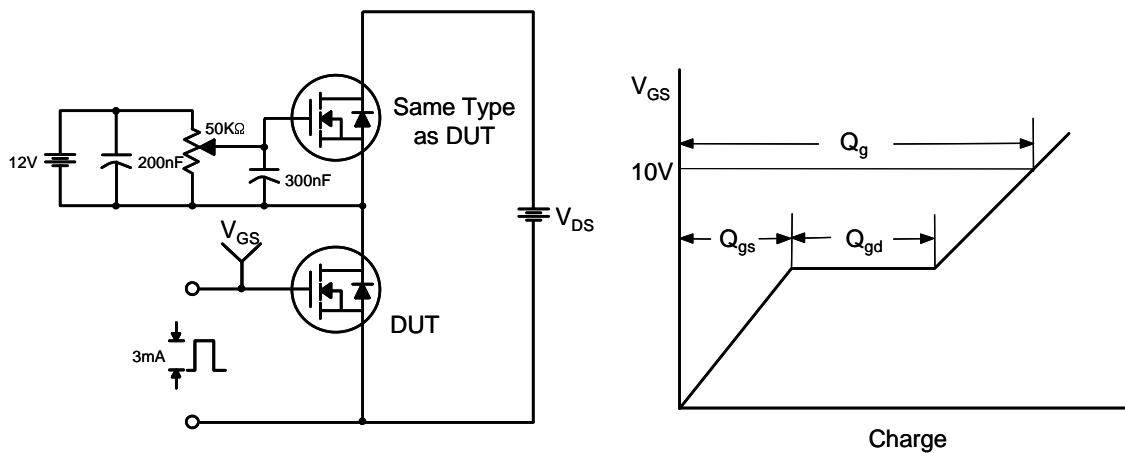
**Figure 10. Maximum Drain Current vs. Case Temperature**



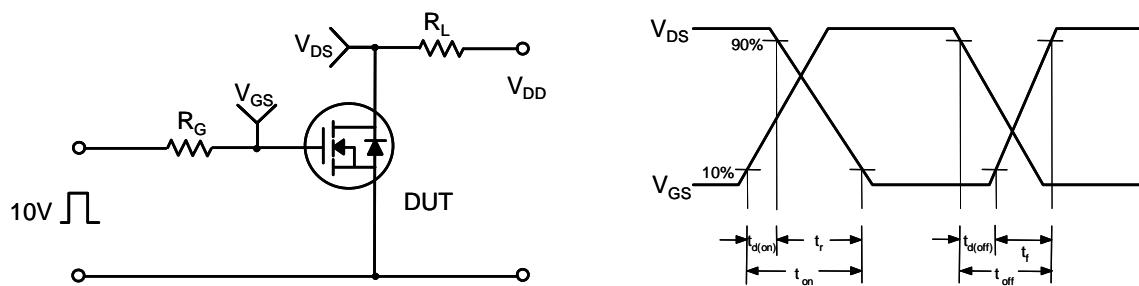
**Figure 11. Transient Thermal Response Curve**



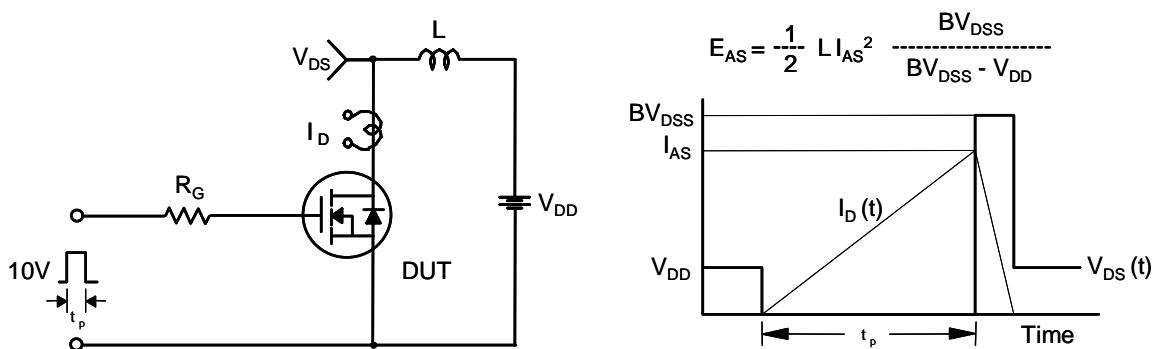
Gate Charge Test Circuit & Waveform



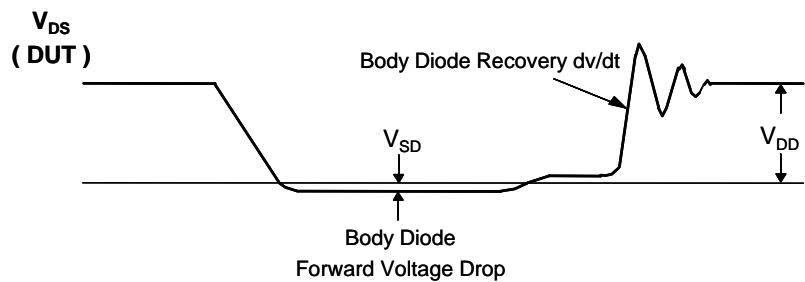
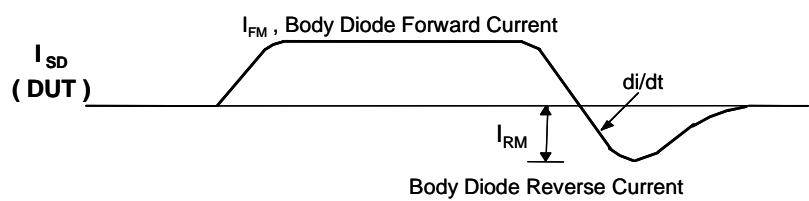
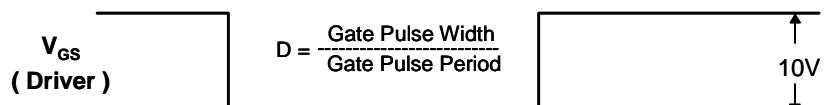
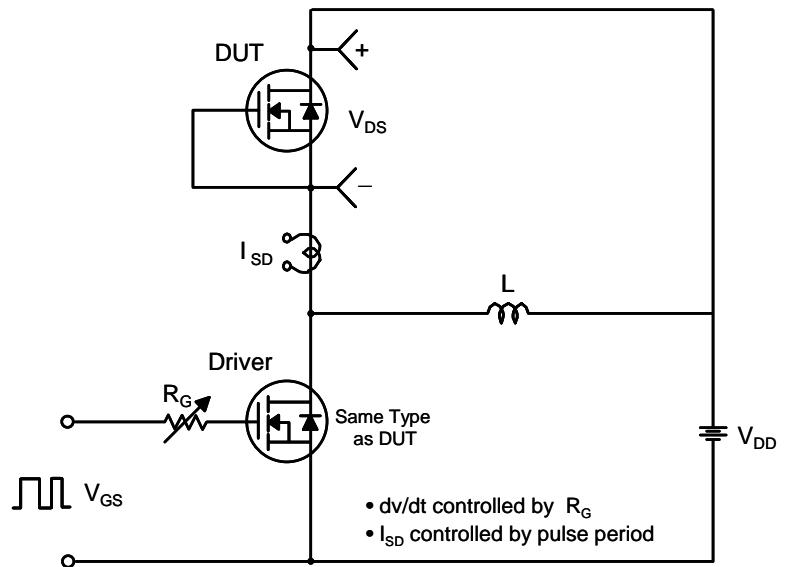
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

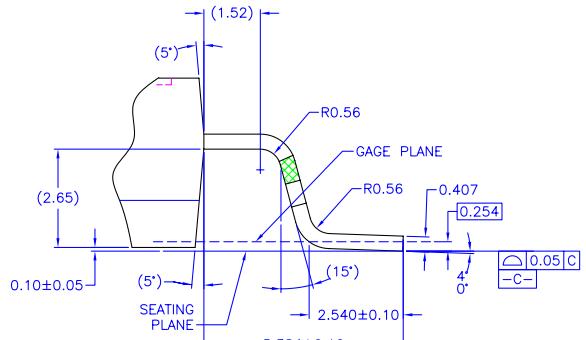
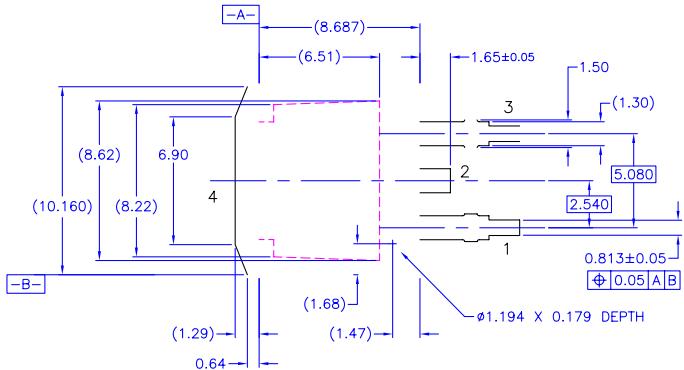


Peak Diode Recovery dv/dt Test Circuit & Waveforms



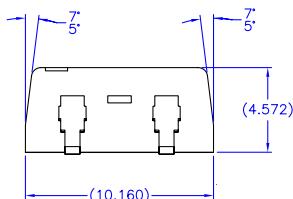
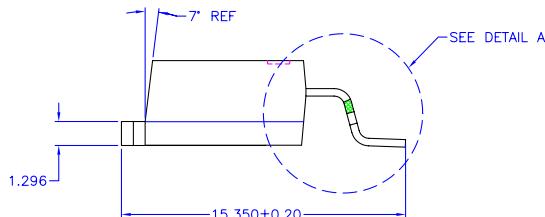
## Mechanical Dimensions

## D2-PAK



DETAIL A

SCALE: 10X



NOTES: UNLESS OTHERWISE SPECIFIED

- A) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICROMETERS MIN.  
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- B) MAXIMUM VERTICAL BURR ON LEAD TIPS NOT TO EXCEED 0.05MM FACING UP.  
VERTICAL LEAD TIP BURR DOWN SHOULD BE ZERO.
- C) NO PACKAGE CHIPS, CRACKS OR SURFACE INDENTATION ALLOWED  
AFTER FORMING.
- D) DOCUMENT REFERENCE:  
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MOLDED PACKAGE: (CB)41-0100, TO-263, 3 LDS, SUZHOU, IDF



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